Digital Blocks Announces DB8051C Microcontroller IP Core

Digital Blocks introduces the DB8051C at the Design Automation Conference (DAC 2009) in San Francisco.

GLEN ROCK, New Jersey, July 31, 2009 – Digital Blocks, a leading developer of silicon-proven semiconductor Intellectually Property (IP) soft cores for embedded processor and video system designers, today announces the DB8051C Microcontroller IP Core. The DB8051C IP Core targets systems-on-chip (SoC) ASSP, ASIC, and FPGA designs requiring the industry standard 8051 Microcontroller.

The DB8051C primary design goal is a small VLSI footprint. This small footprint leads to higher speed, lower power implementations in SoC designs.

In addition, the DB8051C CPU and Memory Interface are optimized to provide higher instruction execution performance. This leads to a 5x speed-up over the Intel 8051 Microcontroller. Combined with Digital Blocks low power design guidelines, the DB8051C offers the industry's best 8051 Microcontroller speed – power ratio.

Price and Availability
The DB8051C is available immediately in synthesizable Verilog along with synthesis scripts, a simulation test bench with expected results, datasheet, and user manual. For further information, product evaluation, or pricing, please visit Digital Blocks at http://www.digitalblocks.com

About Digital Blocks
Digital Blocks designs silicon-proven IP cores for technology systems companies, reducing customer's development costs and significantly improving their time-to-volume goals. Digital Blocks is located at 587 Rock Rd, Glen Rock, NJ 07452 (USA).
Phone: +1-201-251-1281; eFax: +1-702-552-1905; Media Contact: info@digitalblocks.com;
Sales Inquiries: info@digitalblock.com; On the Web at www.digitalblocks.com

###