

General Description

The Digital Blocks DB9000AXI-DCI LCD Controller IP Core interfaces a video image in frame buffer memory via the AMBA 3.0 / 4.0 AXI Protocol Interconnect to a 4K and 2K Digital Cinema Initiative (DCI) High Definition TFT LCD panel.

The video image in frame buffer memory can be 8/10/12-bit YCrCb or RGB, with a Color Space Convert to match the source video to the TFT LCD panel requirements.

The DB9000AXI-DCI IP Core can be implemented in an ASIC, ASSP, or FPGA device with optionally an embedded microprocessor, an AMBA AXI Interconnect fabric, and SDRAM Controller for access to frame buffer memory. Typically, the microprocessor is an ARC, ARM, Intel, MicroBlaze, MIPS, NIOS II, OpenSPARC, PowerPC, or Tensilica processor and frame buffer memory is off-chip DDR3 / DDR4 SDRAM.

Figure 1 depicts the system view of the DB9000AXI-DCI LCD Controller IP Core embedded within an integrated circuit device.

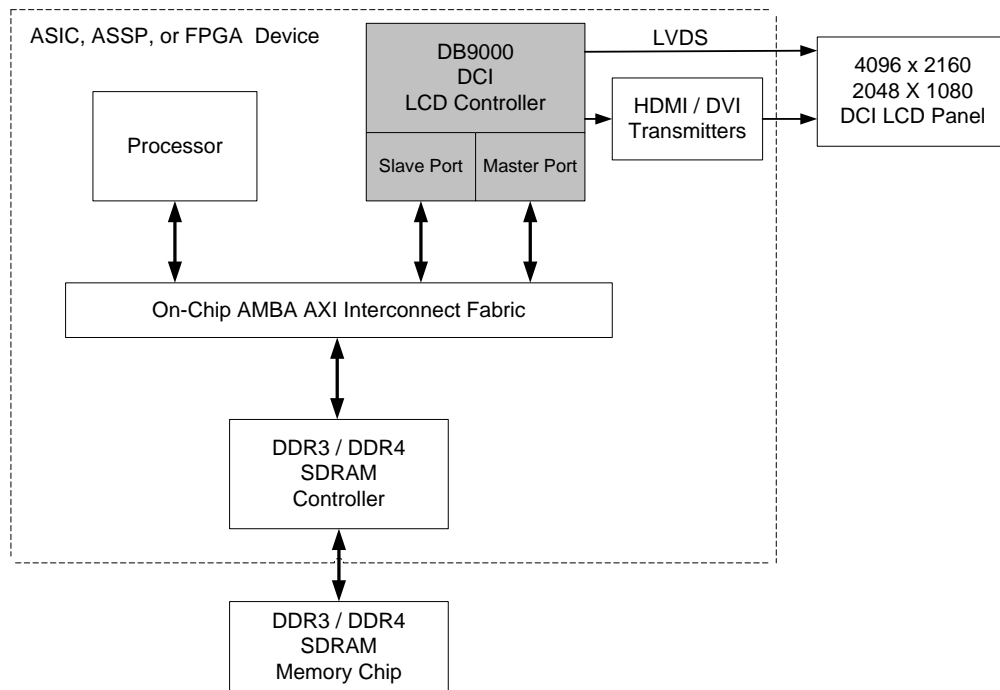


Figure 1: DB9000 DCI LCD Controller – System Diagram

Features

- Digital Cinema Initiative (DCI) formats:
 - 2K – 2048 x 1080 / 12-bit X'Y'Z' / 24/48 frames per second
 - 4K – 4096 x 2160 / 12-bit X'Y'Z' / 24 frames per second
- Additional High Resolution support:
 - 3840 x 2160 Quad / Ultra Full High Definition (QFHD) TFT LCD Panel
- High-Resolution TFT LCD Panel support features by AXI Protocol:
 - Up to 16 overlap outstanding reads requests to the SDRAM Controller
 - Quality of Service (QoS) Support (AXI4)
 - Programmable burst lengths up to 16 beats (AXI3) & 256 beats (AXI4)
 - Wide AXI Master Port data width, up to 256-bits
- Optional Features:
 - Video / Graphics Base Screen with 2-16 Overlay Windows
 - α RGB Alpha Blending
 - Color Space Conversion with Chroma Resampler
- Interface for 1,2, 8 Port TFT LCD Panel:
 - 24-bit digital (8 bits/color) LVDS / CMOS
- Interface to LVDS, DVI, HDMI, & DisplayPort Transmitters / Receivers
- Programmable frame buffer bits-per-pixel (bpp) color depths:
 - 8, 10, 12 bits YCrCb
 - 16, 18, 24 bits RGB
- Color Palette RAM to reduce Frame Buffer memory storage requirements and AXI Bus bandwidth (for lower color applications):
 - 256 entry by 16-bit RAM, implemented as 128 entry by 32-bits
- Programmable horizontal timing parameters:
 - horizontal front porch, back porch, sync width, pixels-per-line
 - horizontal sync polarity
- Programmable vertical timing parameters:
 - vertical front porch, back porch, sync width, lines-per-panel
 - vertical sync polarity
- Programmable pixel clock:
 - pixel clock divider from 1 to 128 of Bus Clock
 - pixel clock polarity
- Programmable Data Enable timing signal:
 - Derived from horizontal and vertical timing parameters
 - display enable polarity
- AMBA AXI4 / AXI3 Interconnect:

- Selectable 256 / 128 / 64 AXI Master Port for DB9000AXI DMA access of frame buffer memory for driving the display
- Selectable 256 / 128 / 64 AXI or AXI4-Lite Slave Port for control & status interface to microprocessor
- Three memories:
 - N-word x 256 / 128 / 64 bit input FIFO, decoupling AXI bus & LCD panel clock rates. Integrated with DMA controller
 - 256-word x 24-bit Color Palette RAM
 - 16-word output FIFO
 - FIFOs parameterizable in depth and width
- Power up and down sequencing support
- 9 sources of internal interrupts with masking control
- Little-endian, big-endian, or Windows CE mode
- AXI4 Bus - Designed to AMBA AXI Protocol Specification (V2.0)
- AXI3 Bus - Designed to AMBA AXI Protocol Specification (V1.0)
- Support in following Integrated Circuits:
 - ASIC / ASSP with AXI4 / AXI3 fabric
 - Altera or Xilinx FPGA with AXI fabric
- Fully-synchronous, synthesizable Verilog RTL core, with rising-edge clocking, No gated clocks, and No internal tri-states.

Block Diagram

Figure 2 depicts the DB9000AXI-DCI LCD Controller IP Core. The controller, with a Video Acquisition Engine, a Base Screen plane + up to 16 Overlay Window video/graphics pixel processor pipelines, and the DCI / Quad FHD Output Formatter, builds on Digital Blocks DB9000 family of TFT LCD Controller IP as well as Video Signal Processing IP library.

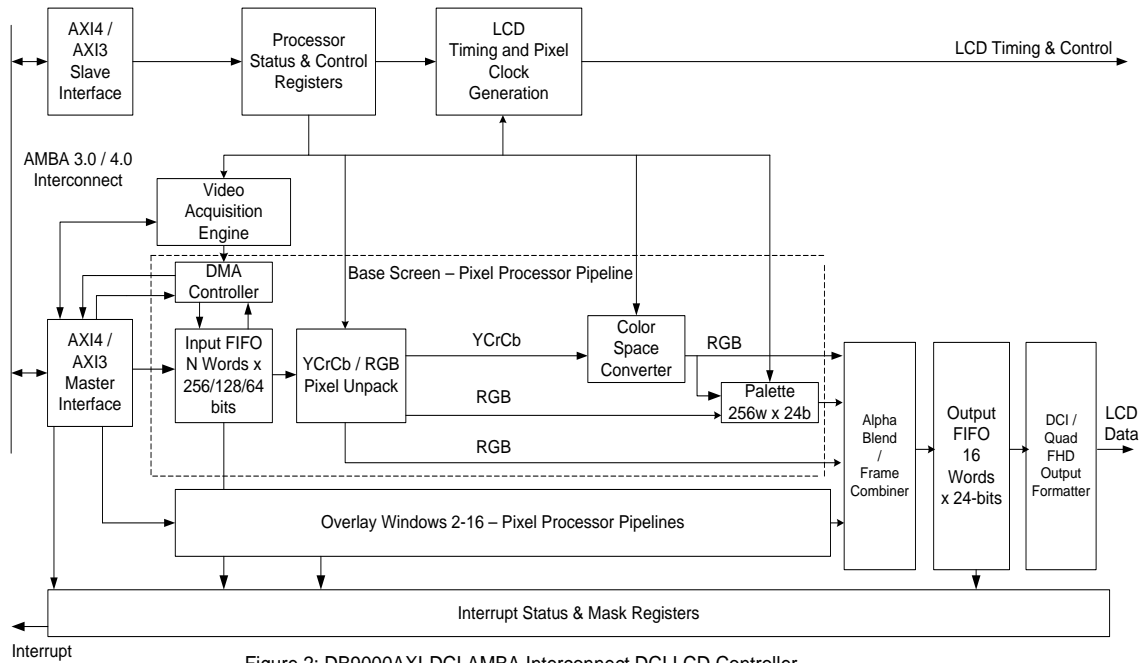


Figure 2: DB9000AXI-DCI AMBA Interconnect DCI LCD Controller

Verification Method

The DB9000AXI-DCI contains a simulation test suite with AXI4 / AXI3 Bus functional models that program the DB9000 control & status registers via the AXI Slave Bus, generates frame buffer data in response to AXI Master requests, and checks expected results.

Customer Evaluation

Digital Blocks offers a variety of methods for prospective customers to evaluate the DB9000AXI-DCI. Please contact Digital Blocks for additional information.

Deliverables

The DB9000AXI-DCI is available in synthesizable RTL Verilog, along with a simulation test bench with expected results, datasheet, and user manual.

Ordering Information

Please contact Digital Blocks for additional technical, pricing, evaluation, and support information.

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