Digital Blocks
Semiconductor IP

# Digital Blocks Qualifies the DB9000 TFT LCD Controller IP Core Family for High Resolution Medical, Industrial, Monitor, and Cinema Applications

*The single DB9000 TFT LCD Controller IP Core in Verilog supports LCD panel resolutions from 240x240 up to 4096x4096.*

**GLEN ROCK, New Jersey, Dec 30, 2010** – Digital Blocks, a leading developer of silicon-proven semiconductor Intellectually Property (IP) soft cores for system-on-chip (SoC) ASIC, ASSP, & FPGA developers with embedded processor & peripherals, networking, display controller, 2D graphics, or video processing requirements, announces the qualification of the DB9000 TFT LCD Controller IP Core to support the most demanding high resolution LCD panels.

"While the DB9000 TFT LCD Controller IP Core has supported 4096x4096 LCD panels from its initial market introduction, over the years, with our customer engagements, we have added features to the DB9000 to support mid range and high resolution LCD panels," said Steven Stein, President of Digital Blocks. "These include 1, 2, & 4 port LVDS interfaces, as well as DVI, HDMI, and DisplayPort interfaces."

The DB9000 IP Core supports SoC / SLI, ASIC, ASSP, & FPGA fabrics interfacing to SDRAM frame buffer memory with 32-, 64-, 128-, or 256-bit data widths, supporting AXI, AHB, Avalon, PLB, and OCP protocols. With respect to the AXI protocol, the DB9000 supports multiple outstanding memory requests, supporting the most demanding, highest resolutions panels.

Support for high resolution LCD panels includes Cinema Scope HD 2560 x 1080, Digital Cinema Systems (DCI) 2048 x 1080 2K image and 4096 x 2160 4K image resolutions, and 10 M Pixel 4096 x 2560 resolution panels. A complete listing follows:

| Format | Resolution |
|---|---|
| Square | 240 x 240 |
| QVGA | 240 x 320 |
| | 240 x 400 |
| | 320 x 240 |
| 16:9 Aspect Ratio | 480 x 234 |
| | 480 x 272 |
| VGA | 480 x 640 |
| | 640 x 480 |
| WVGA | 480 x 800 |
| | 800 x 480 |
| SVGA | 800 x 600 |
| 960x540 | 960 x 540 |
| WSVGA | 1024 x 576 |
| | 1024 x 600 |
| XGA | 1024 x768 |
| SXGA | 1280 x 1024 |
| HD / WXGA | 1366 x 768 |
| WXGA+ | 1440 x 900 |

| Format | Resolution |
|--------|------------|
| HD+ | 1600 x 900 |
| UXGA | 1600 x 1200 |
| WSXGA+ | 1680 x 1050 |
| Full HD | 1920 x 1080 |
| WUXGA | 1920 x 1200 |
| DCI 2K | 2048 x 1080 |
| 3M pixels | 2048 x 1536 |
| CSHD | 2560 x 1080 |
| 5M pixels | 2560 x 2048 |
| 8M pixels | 3840 x 2160 |
| DCI 4K | 4096 x 2160 |
| 10M pixels | 4096 x 2560 |

**Price and Availability**

The DB9000 TFT LCD Controller IP Core family is available in synthesizable Verilog / VHDL, along with a simulation test bench with expected results, datasheet, and user manual. For further information, product evaluation, or pricing, please go to Digital Blocks at http://www.digitalblocks.com

**About Digital Blocks**

Digital Blocks designs silicon-proven IP cores for technology systems companies, reducing customer's development costs and significantly improving their time-to-volume goals. Digital Blocks is located at 587 Rock Rd, Glen Rock, NJ 07452 (USA). Phone: +1-201-251-1281; Fax: +1- 702-552-1905; Media Contact: info@digitalblocks.com; Sales Inquiries: info@digitalblock.com; On the Web at www.digitalblocks.com