General Description

The Digital Blocks DB1830 CCIR 656 Encoder IP Core encodes 4:2:2 Y'CbCr component digital video with synchronization signals to conform to NTSC & PAL video ITU-R BT.656 digital coding standard.

Figure 1 depicts the DB1830 CCIR 656 Encoder IP Core embedded within an integrated circuit device. The DB1830 accept CCIR ITU-R BT.601 4:2:2 sampled Y'CbCr color digital components and synchronization signals and encodes as an NTSC or PAL CCIR BT.656 frame. Control & Status can be programmed into optional DB1830 registers via a bus interface, or set as non-register fixed parameters at synthesis for a smaller VLSI footprint.

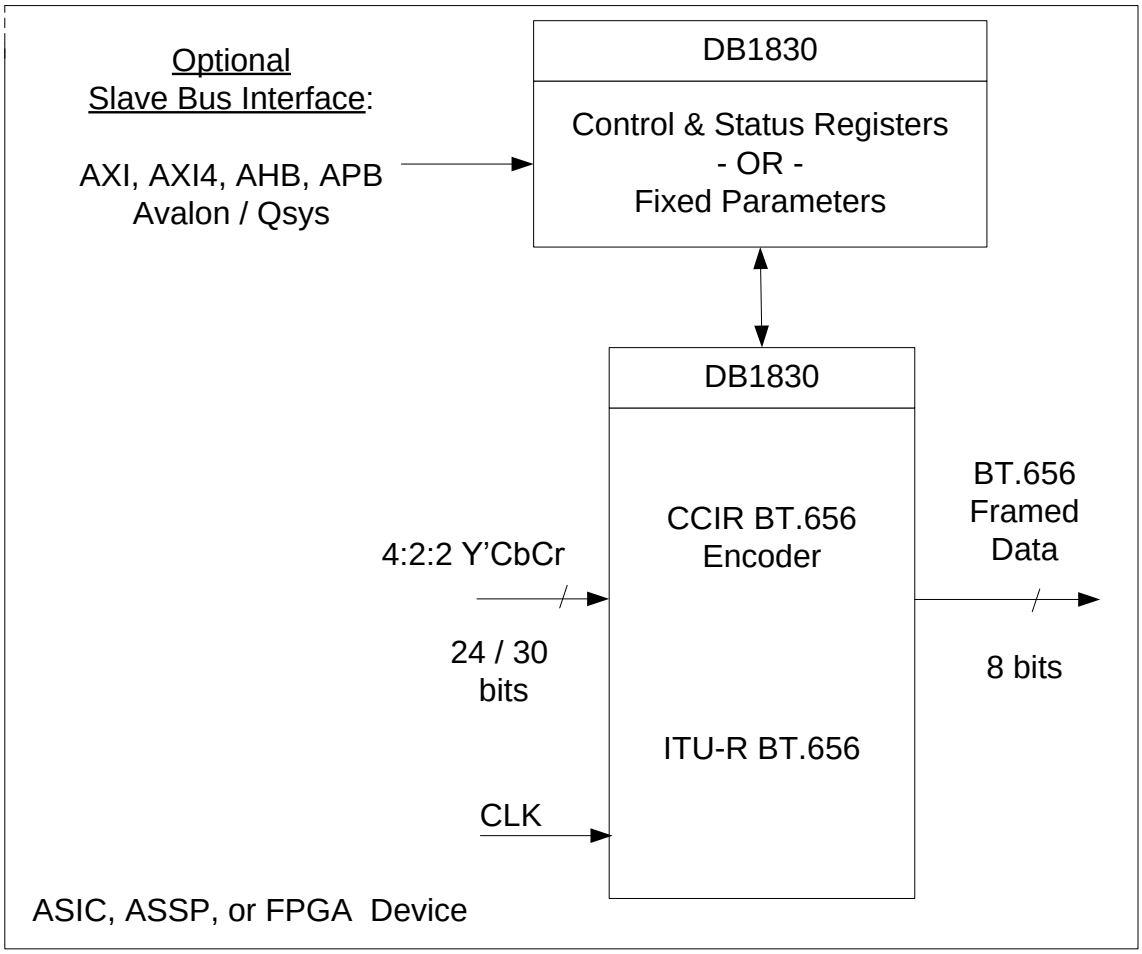
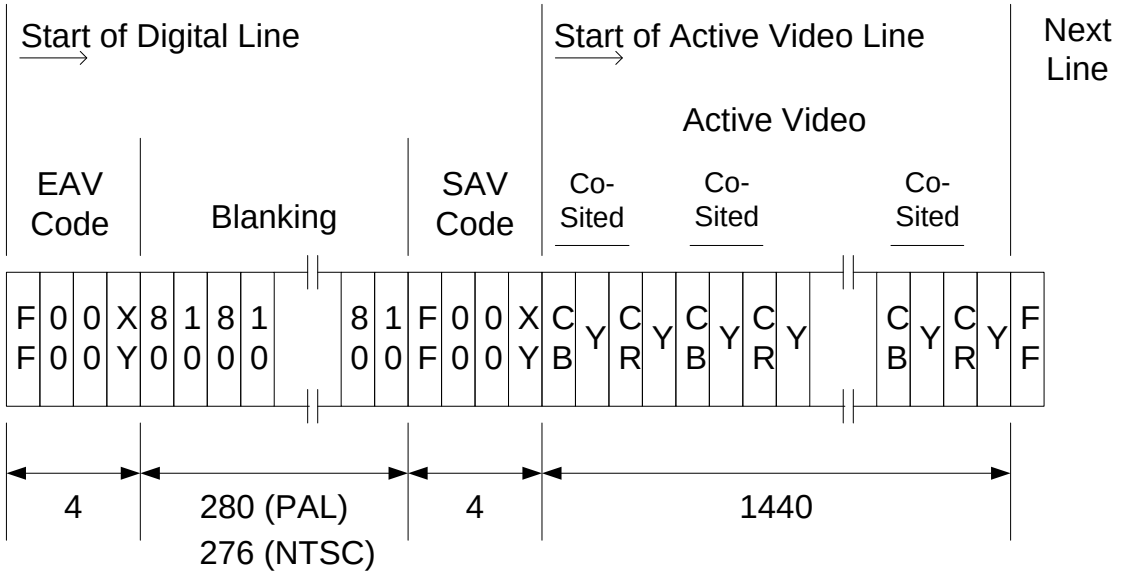


Figure 1: DB1830 CCIR 656 Encoder

DB1830 – BT.656 Encoder

The Digital Blocks DB1830 ITU-R BT.656 Encoder frames the YCbCr 4:2:2 CCIR ITU-R BT.601 digital components within a BT.656 frame which includes End-of-Active Video (EAV), Blanking, and Start-of-Active-Video (SAV) sequence codes.



Features

- Complies with CCIR ITU-R BT.656 specification
- Input CCIR ITU-R BT.601 4:2:2 sampled Y'CbCr color digital components and VSYNC, HSYNC synchronization signals
- Optional 24-bit / 30-bit Y'CbCr components or multiplexed 8-bit Y'CbCr. 8- or 10-bits per component at 27 MHz
- Support BT.656 encoding to NTSC 60 Hz / 525 lines or PAL 50 Hz / 625 lines
- CCIR 656 Encoder - Y'CbCr framed within EAV, Blanking, SAV, XYencoding
- User optional Slave Bus Interface for programming Control & Status Registers
- Member of Digital Blocks' *Video Signal & Image Processing IP Core Family*, which include the following:
    - DB1800 - Standard Definition NTSC/PAL/SECAM Video Sync Separator
    - DB1810 - Color Space Convert
    - DB1820 - Chroma Resampler
    - DB1825 - RGB to YCrCb Color Space Convert with 4:4:4 to 4:2:2 Chroma Resampler
    - DB1830 – CCIR BT.656 Encoder
    - DB1840 – CCIR BT.656 Decoder
    - DB1892 - RGB to CCIR601/656 Encoder
- On-Chip Interconnect Compliance (optional) – Avalon/Qsys, AXI, AXI4, AHB:
    - Avalon Interface Specification (MNL-AVABUSREF-2.0)
    - AMBA AXI Protocol Specification (V1.0)
    - AMBA AXI4 Protocol Specification (V3.0)
    - AMBA AHB Specification 2.0
    - AMBA APB Specification 2.0
- FPGA Integration Support:
    - Altera Quartus II & Qsys / SOPC Integration & NIOS II EDS Reference Design
    - Xilinx ISE Design Suite utilizing AMBA AXI4 & Embedded Development & Software Development Kits
- ASIC / ASSP Design-In Support:
    - Compliance to RTL Design & Coding Standards
    - Digital Blocks Support Services
- Fully-synchronous, pipelined architecture, synthesizable Verilog RTL core

Pin Description

DB1830 CCIR 656 Encoder contains optional AMBA bus AXI, AXI4, AHB, APB and Avalon / Qsys bus for processor programming of internal parameters. The DB1830 optionally contains no bus interface with hard-coding of the video transformation parameters.

The DB1830 contains the following I/O interface. For information on a bus fabric interface I/O, please contact Digital Blocks.

Name	Type	Description
Input Interface		
BT656_PCLK	Input	BT656 Sample Clock
BT656_ PRESETN	Input	BT656 Reset
BT656_VS	Input	BT656 Vertical Sync
BT656_HS	Input	BT656 Horizontal Sync
BT656_YCRCB_VALID	Input	BT656 VALID
BT656_YCRCB_DATAI	Input	BT656 Y'CbCr Data (Mux Input)
Output Interface		
BT656_CLKO	Output	BT656 Encoder Output Clock
BT656_YCRCB_DATAI	Output	BT656 Encoder Output (8/10-bits)

Table 1: DB1830 – I/O Pin Description of CCIR 656 Encoder

Verification Method

The DB1830 contains a test suite with bus functional models that program the DB1830 control & status registers, drives the DB1830 with various standard component color data, and checks expected results.

Customer Evaluation

Digital Blocks offers a variety of methods for prospective customers to evaluate the DB1830. These include Verilog simulations, encrypted FPGA models, or the DB1830 Demo System, which includes an Altera FPGA and 320x240 TFT LCD panel.

Deliverables

The DB1830 is available in FPGA netlist or synthesizable RTL Verilog, along with Synopsys Design Constrains, a simulation test bench with expected results, reference design, and user manual.

Support

The DB1830 IP Core is warranted against defects. One year of phone and email technical support is included, starting with the first interaction. Additional maintenance and support options are available.

Ordering Information

Please contact Digital Blocks for additional technical, pricing, evaluation, and support information.

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