Digital Blocks
Semiconductor IP

DB1800 NTSC/PAL/SECAM Video Sync Separator

General Description

The Digital Blocks DB1800 Video Sync Separator IP Core extracts timing information from a standard NTSC/PAL/SECAM composite sync video signal. The DB1800 extracts horizontal sync, vertical sync, chroma burst / back porch, and field 1 (odd) or field 2 (even) detection from a composite sync input.

Features

The DB1800 contains the following features:

- Auto-detect of Standard Definition (SD) NTSC, PAL, or SECAM video signal.
- Output of following signals:
  - horizontal sync
  - vertical sync
  - chroma burst / back porch
  - field 1 (odd) / field 2 (even) detection
  - display enable for each active video line
- Available in parameterized, synthesizable Verilog RTL. Fully synchronous, single clock design, with asynchronous reset and without internal tri-states.

Applications

- NTSC/PAL/SECAM VLSI Video Decoders
- Broadcast & Professional Video Equipment
- Set-Top Boxes & Digital Video Recorders
- Digital Projector
- Frame Grabber
- LCD/Plasma-TV Panels
- Genlock Circuits

Pin Description

Name	Type	Polarity	Description
resetn	In	Low	Power-up Reset
clk	In	Falling Edge	Clock
csync	In	-	Composite sync
hsync	Out	Low	Horizontal Sync
vsync	Out	Low	Vertical Sync
cburst_blanking	Out	Low	Chroma Burst / Back Porch
field1odd_field2even	Out	High– Field1 Low– Field2	Field1 (odd) / Field2 (even)
display_enable	Out	High	Active Video Line Display Enable

Table 1: DB1800 NTSC/PAL/SECAM Video Sync Separator I/O Pin Description

Functional Description

The DB1800 IP Core NTSC timing for end of Field 2, beginning of Field 1 is depicted in Figure 1. NTSC timing for end of Field 1, beginning of Field 2 is depicted in Figure 2.

Likewise, the PAL/SECAM timing for end of Field 2, beginning of Field 1 is depicted in Figure 3. PAL/SECAM timing for end of Field 1, beginning of Field 2 is depicted in Figure 4.

The five signals depicted in Figures 1 through 4 are CLK, CSYNC, HSYNC, VSYNC, CBURST_BLANKING, FIELD1ODD_FIELD2EVEN, and DISPLAY ENABLE. They are described further below.

CLK

The CLK must be derived from a PLL with the DB1800 HSYNC output as its reference. Either a VLSI PLL or a commercially available Genlock IC is required. Example frequencies are in Table 2.

Function	3 Fsc	CCIR 601 (13.5 MHz)	Square	4Fsc	CCIR 601 (27 MHz)
PAL Fosc (MHz)	13.301	13.5	14.75	17.734	27
NTSC Fosc (MHz)	10.738	13.5	12.273	14.318	27

Table 2: DB1800 Example Input Frequencies

HSYNC (Horizontal Sync)

The HSYNC circuit senses the CSYNC leading edge and generates the true horizontal sync pulse with nominal width of 5.2 microseconds. The HSYNC leading edge is a combinational logic delay of the CSYNC leading edge, important for the external PLL genlock circuit. Once the HSYNC circuit detects the horizontal sync pulse, the next horizontal sync pulse detection is inhibited for 55 % into the horizontal line period. This allows for elimination of the 2H equalization pulses during the vertical blanking period.

Vertical Sync

The VSYNC outputs low during the vertical serration pulses and remains low for a nominal 190 microseconds for a NTSC signal and nominal 128 microseconds for PAL/SECAM.

Chroma Burst / Back Porch Blanking

The Chroma Burst / Back Porch Blanking signal goes active low 200 ns typically after the rising edge of HSYNC and remains low for 3.5 us typically. The Chroma Burst signal can be used to either retrieve the chroma burst form the composite sync signal or as a clamp for the DC restoration of the video waveform.

Field 1 (odd) or Field 2 (even) Detect

NTSC video signals have the half line at the end of Field 1 and start of Field 2. PAL and SECAM signals have the half line at the end of Field 2 and start of Field 1. Thus, a NTSC and PAL/SECAM standard detect function is integral to Field 1 or Field 2 detection. The Field 1 or Field 2 output signal transitions coincident with VSYNC going low, and is high for Field 1 (display odd lines) and low for Field 2 (display even lines). The field detection signal is useful for de-interlacing of interlaced NSTC/PAL/SECAM signals.

Display Enable

Display Enable is high during active video lines. For NTSC, these are video lines 21 through 262 ½ for Field 1 and 283 to 525 for Field 2. For PAL and SECAM, these are lines 23 through 310 for Field 1 and lines 336 through 622 ½ for Field 2. In addition, Display Enable is high only during the active video segment of a horizontal line.

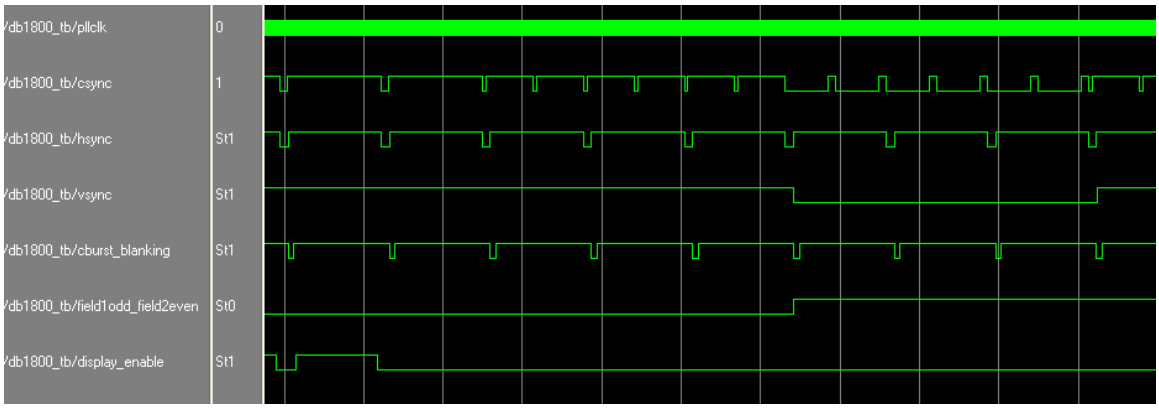

Figure 1: DB1800 - NTSC Timing Diagram – End of Field 2, Start of Field 1

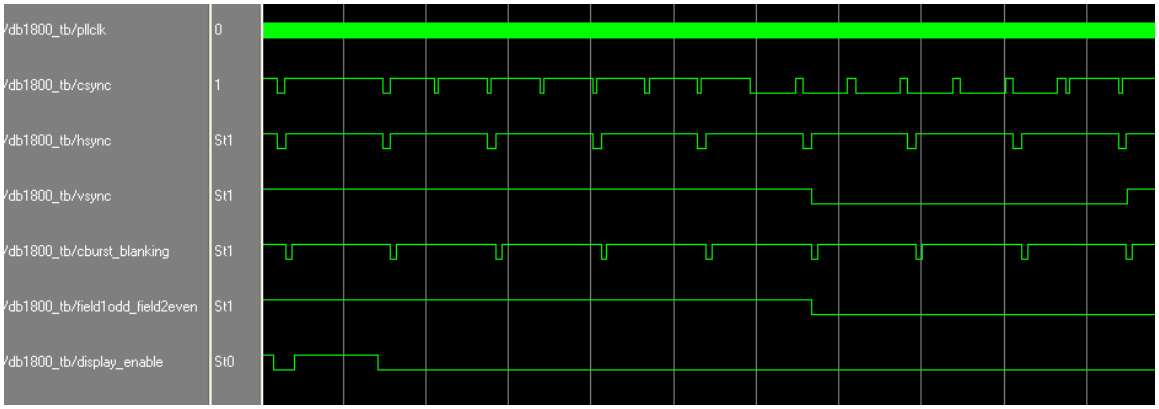

Figure 2: DB1800 - NTSC Timing Diagram - End of Field 1, Start of Field 2

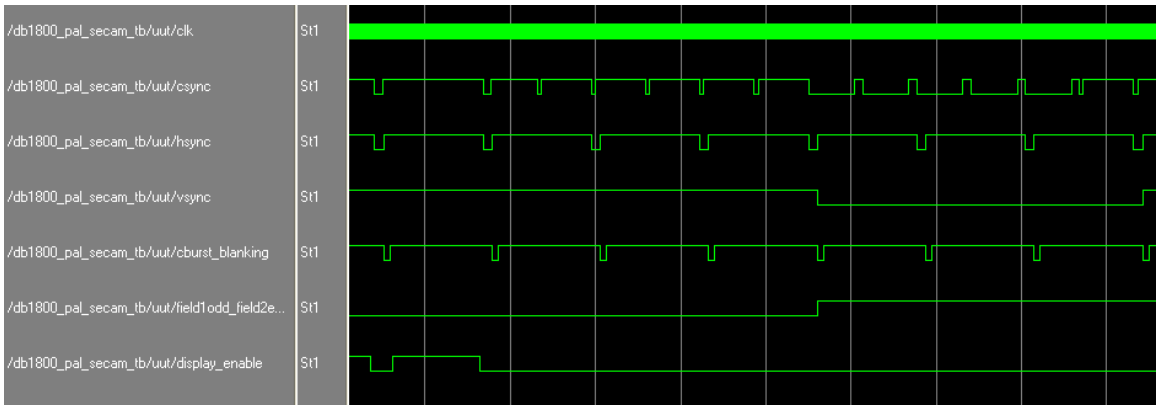

Figure 3: DB1800 – PAL/SECAM Timing Diagram – End of Field 2, Start of Field 1

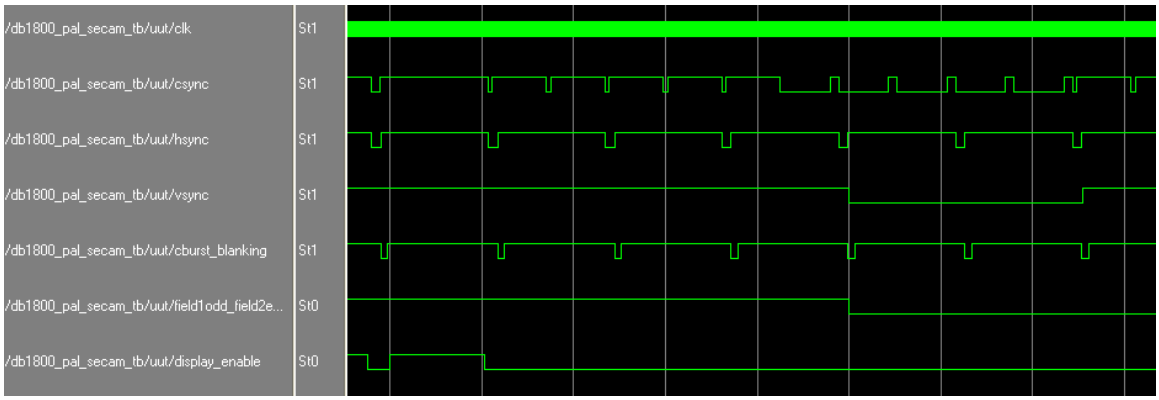

Figure 4: DB1800 – PAL/SECAM Timing Diagram – End of Field 1, Start of Field 2

Verification Methods

The DB1800 NTSC/PAL/SECAM Video Sync Separator IP Core function has been verified in silicon via customer design.

Deliverables

The DB1800 NTSC/PAL/SECAM Video Sync Separator is available in synthesizable RTL Verilog source. The IP Core comes with a test suite, synthesis scripts, data sheet, and user manual. The test suite includes a test fixture, test vectors and expected results.

Ordering Information

Please contact Digital Blocks for additional technical, pricing, and support information.

Digital Blocks, Inc.
PO Box 192
587 Rock Rd
Glen Rock, NJ 07452 USA
Phone: +1-201-251-1281
Fax: +1-702-552-1905
info@digitalblocks.com