General Description

The Digital Blocks DB-UDP-IP is a UDP/IP Hardware Stack / UDP Off-load Engine (UOE) with low latency performance targeting 10/100/1000 MbE or 10/40/100 GbE network links. The DB-UDP-IP is a Verilog SoC IP Core targeting Xilinx Artix/Kintex/Virtex/UltraScale and Altera Cyclone/Arria/Stratix FPGAs.

Figure 1 depicts the UDP/IP Hardware Stack SoC IP Core embedded within an Altera / Xilinx FPGA device, connected on one side to a 10/40 Gigabit Ethernet MAC, and on the other side to the user application running on a Host Processor.

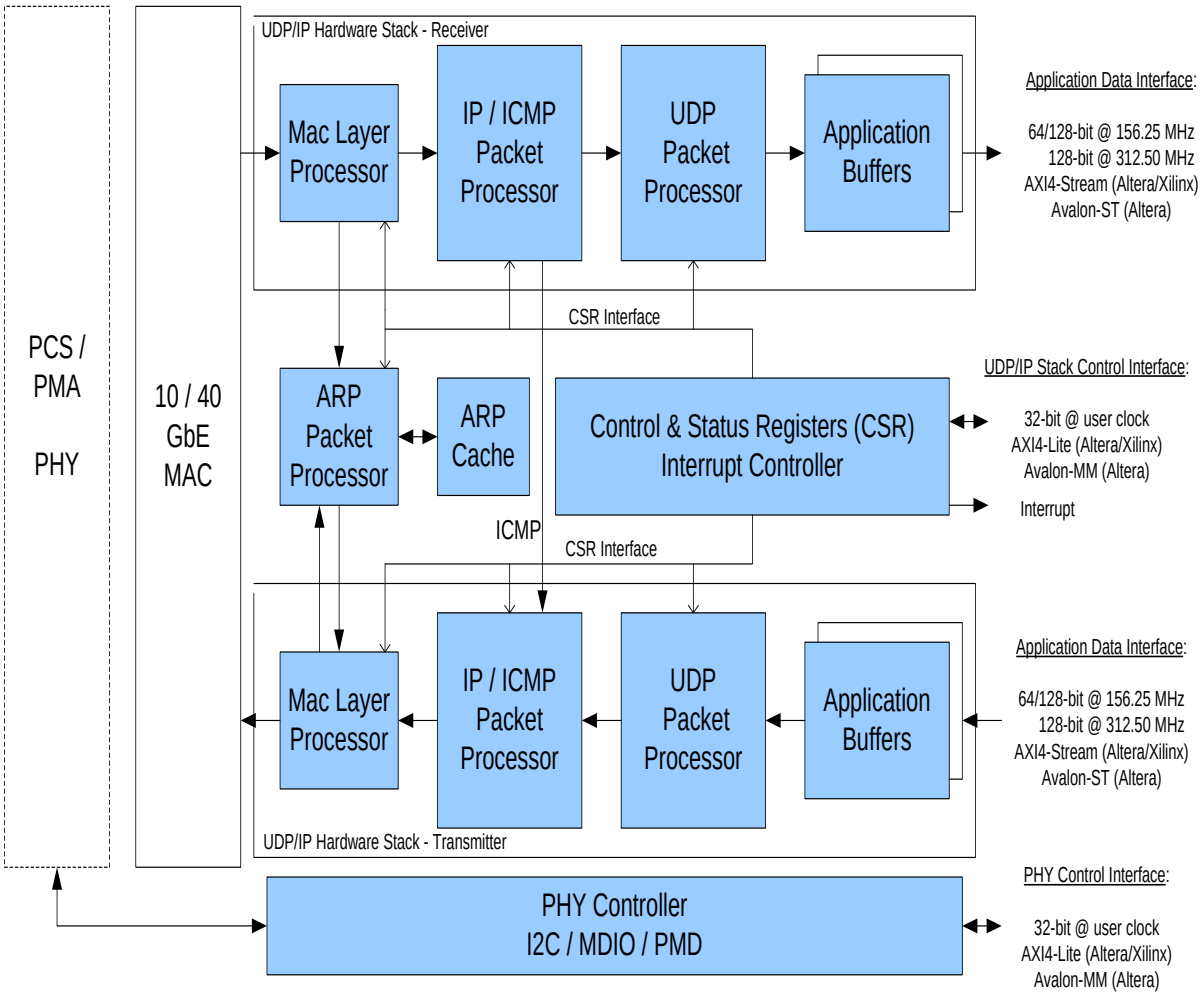

Figure 1: DB-UDP-IP-HFT – UDP/IP Hardware Stack for High Frequency Trading Platforms

Features

- 10/100/1000 MbE or 10/40 GbE wire-line performance with ultra-low latency
- Address Resolution Protocol (ARP) Packet Processor (client/server) with 4-16 entry ARP cache
- VLAN Support
- Internet Protocol (IP) Packet Processor:
    - IP & ICMP (Internet Control Message Protocol) Protocol
    - Host IP address filter, IP header checksum check & generator, user-selectable Maximum Transmission Unit (MTU), Unicast & Multicast Packet support
    - Contact Digital Blocks for Compliance with IETF IPv4/IPv6 RFCs
- User Datagram Protocol (UDP) Packet Processor:
    - Support for up to 256 UDP Ports
    - UDP header checksum check & generator
    - Contact Digital Blocks for Compliance with IETF UDP RFCs
- High Speed Data Interface to user Host Application:
    - 10 GbE: 64-bit @ 156.25 MHz AXI4-Stream or Avalon-ST
    - 40 GbE: 128-bit @ 312.50 MHz AXI4-Stream or Avalon-ST
- Host set-up & control via Control & Status Registers and Interrupt Controller
    - 32-bit @ user clock rate AXI4-Lite or Avalon-MM
- PHY Controller – control interface to user Host Application
- Pipeline, High Clock Rate, Low Latency architecture & design
- Fully-synchronous, synthesizable RTL Verilog SoC IP core

Design Services

The Digital Blocks offers design services incorporating the UDP/IP Hardware Stack / UDP Off-load Engine (UOE) SoC IP Core targeting Xilinx or Altera FPGAs. Digital Blocks can design the FPGA as well as the Printed Circuit Board to meet you system-level requirements. Likewise, we work with global design teams incorporating the UOE SoC IP Core into leading-edge network adapter cards with one or more 10/100/1000 MbE or 10/40 GbE network links. Please contact Digital Blocks for additional information.

Customer Evaluation

Digital Blocks offers a variety of methods for prospective customers to evaluate the UDP/IP Hardware Stack UDP Off-load Engine (UOE) SoC IP Core. Please contact Digital Blocks for additional information.

Deliverables

The DB-UDP-IP-HFT IP Core is available in synthesizable RTL Verilog or a technology-specific netlist for FPGAs, along with Synopsys Design Constraints, a simulation test bench with expected results, datasheet, and user manual.

Ordering Information

Please contact Digital Blocks for additional technical, pricing, evaluation, and support information.

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