General Description

The Digital Blocks DB-SPI-S-AMBA is a Serial Peripheral Interface (SPI) Controller Verilog IP Core supporting only Slave SPI Bus transfers (both Full Duplex and Half Duplex). The DB-SPI-S contains an AMBA AXI, AHB, or APB Bus Interface for interfacing a microprocessor to external SPI Slave devices.

The DB-SPI-S contains Transmit/Receive FIFOs and Finite State Machine control with status & interrupt capability to fully off-load from the microprocessor the transfer of data over the SPI Bus. Optionally, the user can transfer transmitted or received data from the SPI Bus to user memory via an optional DMA Controller.

The DB-SPI-S targets ASIC / ASSP / FPGA integrated circuits, where typically, the microprocessor is an ARM processor, but can be any embedded processor. Figure 1 depicts the system view of the DB-SPI-S Controller IP Core embedded within an integrated circuit device.

The DB-SPI-S offers a Microprocessor a SPI Master only function in a smaller VLSI footprint than the DB-SPI-MS Master/Slave version.

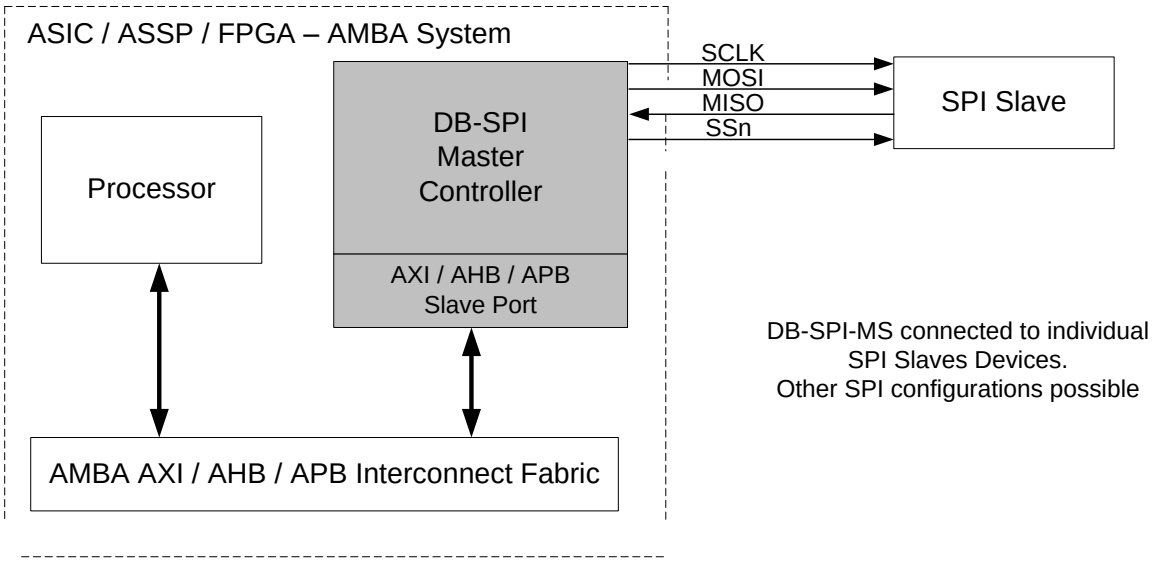

Figure 1: DB-SPI-S Controller – System Diagram

Features

- Slave SPI Modes
- Half Duplex / Full Duplex Transfers – Simultaneous Transmit & Receive
- Four Signal Interface:
  - SO - Slave Output (Data)
  - SI - Slave Input (Data)
  - SCK - Serial Clock
  - SS - Slave Select
- Configurable SPI Modes:
  - Standard SPI Mode (1 Data Lane)
  - Dual SPI Mode (2 Data lanes)
  - Quad SPI Mode (4 Data Lanes)
- Programmable SPI Frame Formats:
  - Programmable Words-Per-Frame (1 to Full Depth of FIFO)
  - Programmable LSB-first or MSB-first Per Word
- Two Clock Domains:
  - AMBA Bus / SCK Clocks
- Separate Transmit / Receive FIFOs:
  - Dual Clock Domains
  - 8- bit Data Width
  - Configurable depth - 4 to 256 Bytes
  - Implemented as Registers or SRAM
- SCK Clock Generator:
  - Programmable SCK Rate
  - Programmable Clock Phase & Polarity
- Optional DMA Controller for transfers between System Memory & SPI Bus
- Internal interrupts with masking control
- Available AMBA Microprocessor Interfaces:
  - AXI / AHB / APB Buses
  - 8 / 16 / 32 bit Data Interface
- Compliance with ARM AMBA and Freescale / Motorola SPI specifications:
- Fully-synchronous, synthesizable Verilog RTL core, with rising-edge clocking, no gated clocks, and no internal tri-states, for easy integration into FPGA or ASIC design flows.

Pin Description

In addition to either of the AMBA AXI / AHB/ APB Bus interfaces, which include the input CLOCK and RESET signals and the output INTR (interrupt) signal, the SPI interface signals are listed in Table 1.

Name	Type	Description
SPI Bus Interface		
MO	Master - Output	Master - Serial Data Output
MI	Master - Input	Master - Serial Data Input
SCK	Master - Output	Master - Serial Clk Output
SS	Master - Output	Master – Slave Select Output

Table 1: DB-SPI-MS – I/O Pin Description

Verification Method

The DB-SPI-M Controller IP Core contains a test suite with AMBA AXI, AHB, APB Bus functional models that program the DB-SPI-M control & status registers, generates & sends SPI data, monitors the SPI bus protocol, and checks expected results.

The DB-SPI-M Controller IP Core has internally been verified as follows:

- Instantiated within an FPGA, controlled by an ARM processor, and communicating with (1) merchant semiconductor devices containing SPI Master & Slave bus interfaces; and (2) FPGAs/ASICs containing SPI Master / Slave bus interfaces in Customer implementations.

Ordering Information

Digital Blocks DB-SPI-M are available as follows:

Digital Blocks Number	AMBA Interface
DB-SPI-M-AXI	AXI Interface – Read/Write Channels
DB-SPI-M-AXI-Lite	AXI Interface – Read/Write Channels (Reduced Signaling)
DB-SPI-M-AHB	AHB Slave Interface – Read/Write
DB-SPI-M-APB	APB Slave Interface – Read/Write

Customer Evaluation

Digital Blocks offers a variety of methods for prospective customers to evaluate the DB-SPI-M. Please contact Digital Blocks for additional information.

Deliverables

The DB-SPI-M is available in synthesizable RTL Verilog or a technology-specific netlist for FPGAs, along with Synopsys Design Constraints, a simulation test bench with expected results, datasheet, and user manual.

The DB-SPI-M comes along with example C code software for controlling Transmit and Receive Transactions in an Eclipse-based ARM Integrated Development Environment (IDE).

Ordering Information

Please contact Digital Blocks for additional technical, pricing, evaluation, and support information.

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