

General Description

The Digital Blocks DB-SPI-MS-AVLN is a Serial Peripheral Interface (SPI) Controller Verilog IP Core supporting both Master/Slave SPI Bus transfers. The DB-SPI-MS contains an Avalon Bus Interface for interfacing a microprocessor to external SPI Master/Slave devices.

The DB-SPI-MS contains Transmit/Receive FIFOs and Finite State Machine control with status & interrupt capability to fully off-load from the microprocessor the transfer of data over the SPI Bus. Optionally, the user can transfer transmitted or received data from the SPI Bus to user memory via an optional DMA Controller.

The DB-SPI-MS targets FPGA integrated circuits, where typically, the microprocessor is a NIOS II or ARM processor, but can be any embedded processor. Figure 1 depicts the system view of the DB-SPI-MS Controller IP Core embedded within an integrated circuit device.

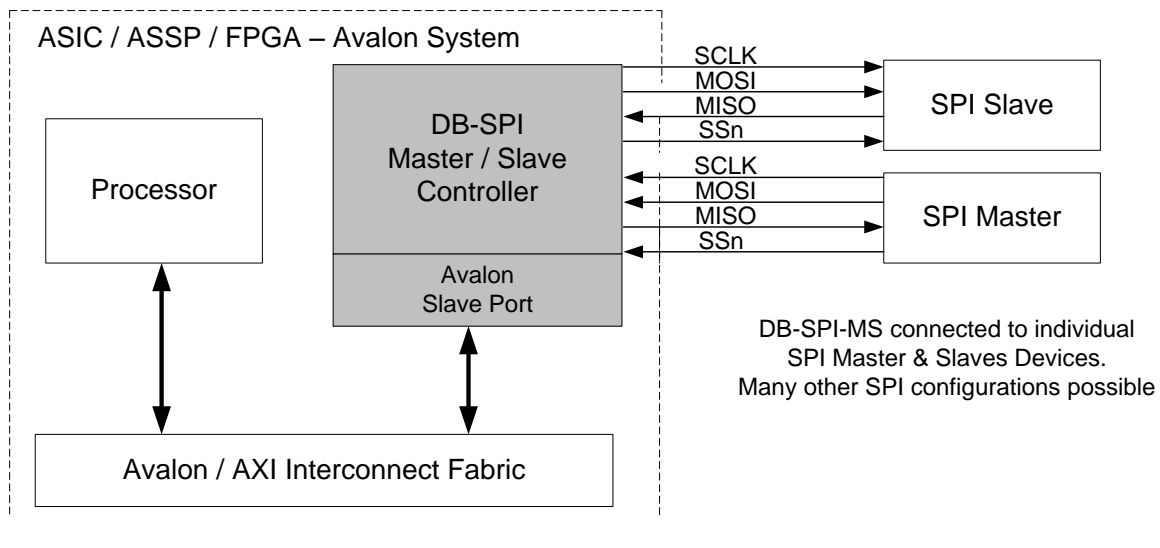


Figure 1: DB-SPI-MS Controller – System Diagram

Within an Altera FPGA, the DB-SPI-MS-AVLN can connect to an Avalon or AXI Interconnect within Quartus II – Qsys, connecting to a NIOS II or ARM SoC microprocessor.

Features

- Master and Slave SPI Modes
- Half Duplex / Full Duplex Transfers – Simultaneous Transmit & Receive
- Four Signal Interface:
 - MOSI - Master Output, Slave Input (Data)
 - MISO - Master Input, Slave Output (Data)
 - SCK - Serial Clock
 - SS[N:0] - Slave Select
- Up to N=8 Slave Select (SS) Outputs for multiple Slaves on SPI Bus
- Configurable SPI Modes:
 - Standard SPI Mode (1 Data Lane)
 - Dual SPI Mode (2 Data lanes)
 - Quad SPI Mode (4 Data Lanes)
- Programmable SPI Frame Formats:
 - Programmable SPI Frame
 - Programmable inter-frame gap
 - Programmable LSB-first or MSB-first frames
- Configurable FIFO depth for off-loading the SPI transfers from the processor:
 - Separate Transmit / Receive FIFOs
- Three Clock Domain Configuration options
- SCK Clock Generator - Master Mode:
 - Programmable SCK Rate
 - Programmable Clock Phase & Polarity
- Optional DMA Controller for transfers between User Memory & SPI Bus
- Internal interrupts with masking control
- Available Avalon Microprocessor Interfaces:
 - 8 / 16 / 32 bit Data Interface
- Available AXI Interconnect for interface to Altera SoC ARM
- Compliance with Freescale / Motorola SPI specifications:
- Fully-synchronous, synthesizable Verilog RTL core, with rising-edge clocking, no gated clocks, and no internal tri-states, for easy integration into FPGA or ASIC design flows.

Pin Description

In addition to either of the Avalon Bus interfaces, which include the input CLOCK and RESET signals and the output INTR (interrupt) signal, the SPI interface signals are listed in Table 1.

Name	Type	Description
SPI Bus Interface		
MOSI	Master - Output	Master - Serial Data Output
	Slave - Input	Slave - Serial Data Input
MISO	Master - Input	Master - Serial Data Input
	Slave - Output	Slave - Serial Data Output
SCLK	Master - Output	Master - Serial Clk Output
	Slave - Input	Slave - Serial Clk Input
SS	Master - Output	Master - Slave Select Output
	Slave - Input	Slave - Serial Select Input

Table 1: DB-SPI-MS – I/O Pin Description

Verification Method

The DB-SPI-MS Controller IP Core contains a test suite with Avalon Bus functional models that program the DB-SPI-MS control & status registers, generates & sends SPI data, monitors the SPI bus protocol, and checks expected results.

The DB-SPI-MS Controller IP Core has internally been verified as follows:

- Instantiated within an FPGA, controlled by a NIOS II processor, and communicating with (1) merchant semiconductor devices containing SPI Master & Slave bus interfaces; and (2) FPGAs/ASICs containing SPI Master / Slave bus interfaces in Customer implementations.

Ordering Information

Digital Blocks DB-SPI-MS are available as follows:

Digital Blocks Number	AMBA Interface
DB-SPI-MS-AVLN	SPI Master/Slave
DB-SPI-M-AVLN	SPI Master Only
DB-SPI-S-AVLN	SPI Slave Only
Contact Digital Blocks for information on AMBA AXI, AHB, APB Interconnect Interfaces	

Customer Evaluation

Digital Blocks offers a variety of methods for prospective customers to evaluate the DB-SPI-MS. Please contact Digital Blocks for additional information.

Deliverables

The DB-SPI-MS is available in synthesizable RTL Verilog or a technology-specific netlist for FPGAs, along with Synopsys Design Constraints, a simulation test bench with expected results, datasheet, and user manual.

The DB-SPI-MS comes along with example C code software for controlling Transmit and Receive Transactions in an Eclipse-based NIOS II Integrated Development Environment (IDE).

Ordering Information

Please contact Digital Blocks for additional technical, pricing, evaluation, and support information.

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