General Description

The Digital Blocks DB-RTP-UDP-IP-MPEG-TS IP Core contains a MPEG Transport Stream (TS) processor with RTP/UDP/IP Protocol Hardware Stack, MAC Layer Pre- & Post-Processors, and an ARP Packet Processor targeting high packet throughput or low latency of MPEG Transport of Audio/Video Packets over a Internet Protocol (IP) Network or storage in memory. The DB-RTP-UDP-IP-MPEG-TS is a Verilog SoC IP Core targeting Xilinx/Altera/Lattice/Microsemi FPGAs and ASIC/ASSP devices.

Figure 1 depicts the MPEG-TS with RTP/UDP/IP Protocol Hardware Stack SoC IP Core embedded within an FPGA/ASSP/ASIC device, connected on one side to a 10/100 MbE or 1/10/40 Gigabit Ethernet MAC, and on the other side to the user application, such as MPEG2-TS.

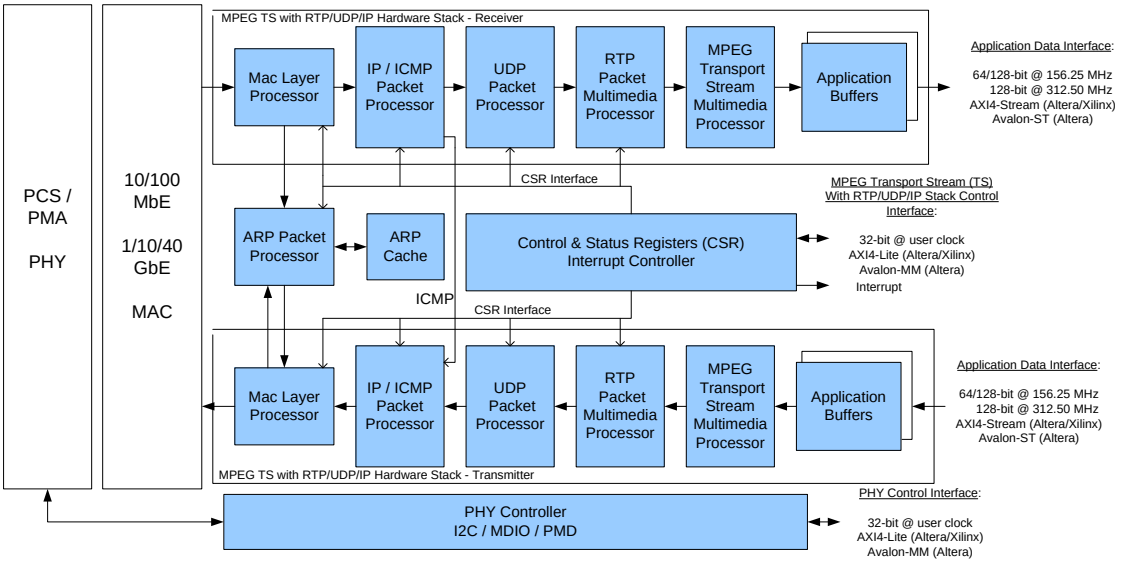

Figure 1: DB-RTP-UDP-IP-MPEG – MPEG Transport Stream with RTP/UDP/IP Hardware Stack for Audio/Video Applications

Features

- Compliance with ISO/IEC 13818-1
- MPEG Transport Stream with programmable RTP Encapsulation (Transmitter) / Decapsulation (Receiver) over UDP/IP Protocols.
- 10/100 MbE as well as 10/40 Gb wire-line performance with either high packet throughput or ultra-low latency Audio/Video data within encapsulated MPEG-Transport Stream / RTP / UDP / IP packet.
- MPEG-TS Optional Configurations:
  - 1, 2, 4, 8, 16 MPEG Transport Streams
  - Encapsulation / Decapsulation for both Transmit & Receive
  - Either Encapsulation or Decapsulation for reduced VLSI footprint
- Address Resolution Protocol (ARP) Packet Processor (client/server) with 4-16 entry ARP cache
- Internet Protocol (IP) Packet Processor:
  - IPv4 and IPv6 (optional) & ICMP (Internet Control Message Protocol) Protocol
  - IP header checksum generator (transmitter) & check (receiver), user-selectable Maximum Transmission Unit (MTU), Unicast, Broadcast & Multicast Packet support
  - Compliance with IETF IPv4/IPv6 RFCs
- User Datagram Protocol (UDP) Packet Processor:
  - Support for 1, 2, 4, 8, 16 UDP Ports
  - UDP header checksum generator (transmitter) & check (receiver)
  - Compliance with IETF UDP RFCs
- Real Time Transport Protocol (RTP) Packet Processor
  - Encapsulates (transmitter) /Decapsulates (receiver) MPEG-TS within RTP packets
  - Compliance with IETF RTP RFCs
- High Speed Data Interface to user Host Application:
  - 10 GbE: 64-bit @ 156.25 MHz AXI4-Stream or Avalon-ST
  - 40 GbE: 128-bit @ 312.50 MHz AXI4-Stream or Avalon-ST
- Host set-up & control via Control & Status Registers and Interrupt Controller
  - 32-bit @ user clock rate AXI4-Lite or Avalon-MM
  - Optional hardwired setup
- Pipeline, High Clock Rate, Low Latency architecture & design
- Fully-synchronous, synthesizable RTL Verilog SoC IP core

Customer Evaluation

Digital Blocks offers a variety of methods for prospective customers to evaluate the RTP/UDP/IP Protocol Hardware Stack SoC IP Core. Please contact Digital Blocks for additional information.

Deliverables

The DB-RTP-UDP-IP-MPEG-TS IP Core is available in synthesizable RTL Verilog or a technology-specific netlist for FPGAs, along with Synopsys Design Constraints, a simulation test bench with expected results, datasheet, and user manual.

Ordering Information

Please contact Digital Blocks for additional technical, pricing, evaluation, and support information.

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