General Description

The Digital Blocks DB-I2C-S-Hs-Mode I2C Slave Controller IP Core interfaces a microprocessor via the AMBA AXI / AHB / APB Bus or Avalon Bus to an I2C Bus in Hs-Mode (3.4 Mbit/s) / Ultra Fast-Mode (5 Mbit/s) / Fast-Mode Plus (1 Mbit/s) / Fast-Mode (400 Kbit/s) / Standard-Mode (100 Kbit/s).

The I2C is a two-wire bidirectional interface standard (SCL is Clock, SDA is Data) for transfer of bytes of information between two or more compliant I2C devices, typically with a microprocessor behind the master controller and one or more slave devices.

The DB-I2C-S-Hs-Mode is a Slave I2C Controller that implements the Slave-Transmit and Slave-Receive protocol according to the Philips I2C-Bus Specification, Version 2.1 as well as the updated NXP UM10204 Rev 6 – 4 April 2014 Specification.

Figure 1 depicts the system view of the DB-I2C-S-Hs-Mode Slave Controller IP Core embedded within an ASIC, ASSP or FPGA device. The DB-I2C-S-Hs-Mode Controller receives and transmits data with respect to an external I2C Master Controller. The DB-I2C-S-Hs-Mode can interface to a user Registers, Memory, Peripheral, or CPU.

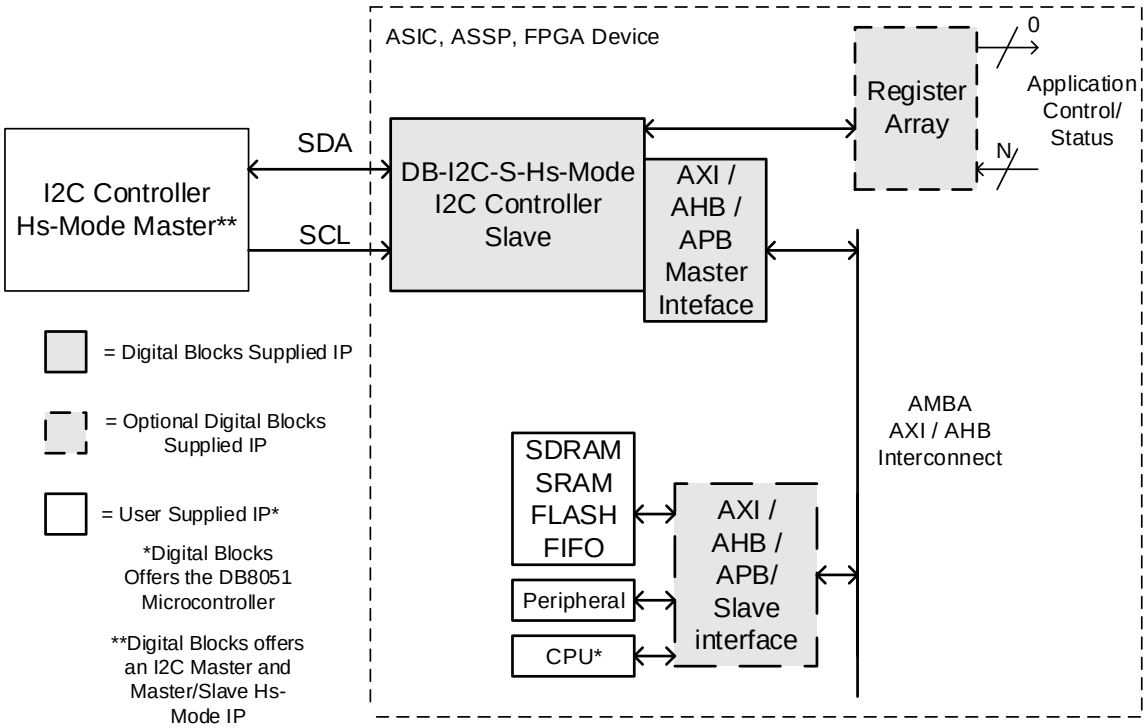

Figure 1: DB-I2C-S-Hs-Mode Slave Controller - System View

The DB-I2C-S-Hs-Mode IP Core can function standalone, without the requirement for an embedded processor.

Features

- Slave I^2C Controller Modes:
  - Slave–Transmitter
  - Slave–Receiver
- Supports following I2C bus speeds:
  - Hs-Mode (3.4+ Mb/s)
  - Ultra Fast-Mode (5 Mb/s)
  - Fast Mode Plus (1 Mb/s)
  - Fast Mode (400 Kb/s)
  - Standard Mode (100 Kb/s)
- I2C compliant features:
  - Repeated Start, 7/10-bit addressing, General Call, SCL Low Wait States
- Parameterized FIFO memory for off-loading the I^2C transfers from the processor:
  - Targets embedded processors with higher performance algorithm requirements, by the I^2C Controller independently controlling the Transmit or Receive of bytes of information buffered to and from a FIFO.
- System-level features & integration capabilities:
  - CPU Interface via parameterized FIFO with support for APB / AHB / AXI / AXI-lite / Avalon SoC Iinterconnect fabrics
  - Enhanced SCL / SDA spike filtering capabilities
  - Enhanced Repeated Start capabilities
- Optional system-level features & integration capabilities:
  - DMA transfer between the I2C Bus & Memory (SDRAM / SRAM / FLASH)
  - Direct interface to user Registers within ASIC / ASSP / FPGA device, for Master/Slave transfer across the I2C Bus
  - Remote Configuration of a Digital Blocks' I2C Slave by an I2C Master
  - SMBus Support:
    - SMBus Timeout
    - SMBus Alert
    - SMBus Data minimum hold time
- 13 sources of internal interrupts with masking control
- Compliance with I2C specifications:
  - Compliance with AMBA AXI / AHB/ APB Protocol Specifications
  - Philips – The I2C-Bus Specification, Version 2.1, January 2000
  - NXP UM10204 Rev 6 – 4 April 2014
- Fully-synchronous, synthesizable Verilog RTL core, with rising-edge clocking, no gated clocks, and no internal tri-states, for easy integration into FPGA or ASIC design flows.

Digital Blocks offers I2C Master/Slave, Master-only, and Slave-only Controller IP supporting Hs-Mode / Fast Mode Plus / Fast Mode / Standard Mode.

Pin Description

The DB-I2C-S-Hs-Mode I2C Slave Controller interface signals are listed in Table 1.

Name	Type	Description
I2C Bus Interface		
SDAI	Input	Serial Data
SDAO	Output	Serial Data
SCLI	Input	Serial Clock Line
Register Array / SRAM / FIFO / AMBA / Avalon Interface		
Please contact Digital Blocks for more information		

Table 1: DB-I2C-S-Hs-Mode – I/O Pin Description

Verification Method

The DB-I2C-S-Hs-Mode Controller IP Core contains a verification test suite that generates & sends I2C transactions, monitors the I2C bus protocol, and checks expected results.

The DB-I2C-S-Hs-Mode Controller IP Core has internally been verified as follows:

- Instantiated within an FPGA, and communicating with NXP I2C Master IP Controller, and an ARM processor within the FPGA for expected data checking.
- I2C Bus Compliance testing with lab instrumentation.
- Customer Implementations.

Customer Evaluation

Digital Blocks offers a variety of methods for prospective customers to evaluate the DB-I2C-S-Hs-Mode. Please contact Digital Blocks for additional information.

Deliverables

The DB-I2C-S-Hs-Mode is available in synthesizable RTL Verilog or a technology-specific netlist for FPGAs, along with Synopsys Design Constraints, a simulation test bench with expected results, datasheet, and user manual.

Ordering Information

Please contact Digital Blocks for additional technical, pricing, evaluation, and support information.

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