General Description

The Digital Blocks DB-I2C-S Controller IP Core implements an I2C Slave Controller, with a user parameterized Register Array or Memory (SDRAM / SRAM / Flash / FIFO) or any Peripheral or CPU connecting on an internal AHB / APB / AXI / Avalon / Qsys Bus for embedded user I/O Control & Status or block data transfers with an ASIC / ASSP / FPGA device. The DB-I2C-S Controller implements the Slave-Transmit and Slave-Receive protocol according to the Philips I2C-Bus Specification, Version 2.1 as well as the updated NXP Rev .5 October 9, 2012 Specification.

Figure 1 depicts the system view of the DB-I2C-S Controller IP Core embedded within an ASIC, ASSP or FPGA device. The DB-I2C-S Controller receives and transmits data with respect to an external I2C Master Controller. The DB-I2C-S can interface to a user Register Array, Memory such as SRAM, SRAM, Flash, or a FIFO, or an AXI / AHB / APB / Avalon / Qsys Interface to a Peripheral or CPU.

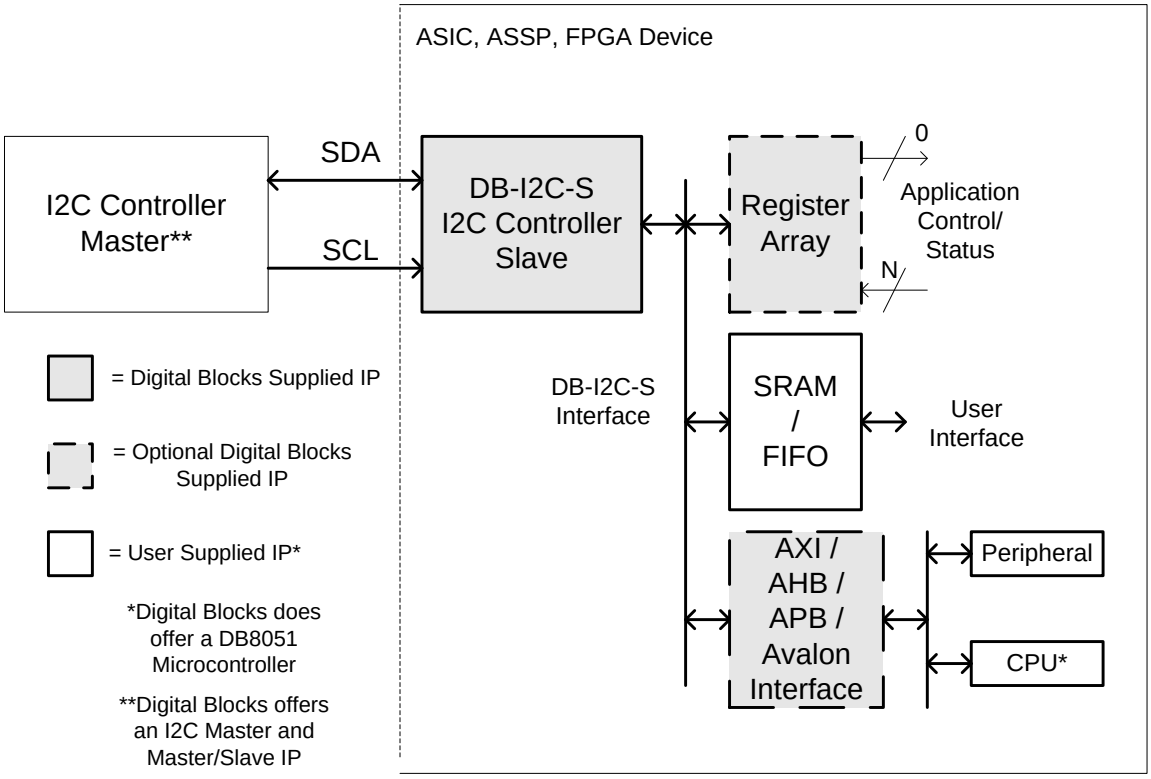

Figure 1: DB-I2C-S Controller - System View

For the Register Array, the number of user registers is parameterized and the DB-I2C-S provides an auto-increment mode whereby an I2C bus transaction with multiple bytes can

be written to or read from the registers. The DB-I2C-S IP Core can function standalone, without the requirement for an embedded processor.

Features

- I2C Slave Controller - Implements Slave-only protocol for smaller VLSI footprint, for applications requiring Slave–Receiver and Slave–Transmitter capability
- DB-I2C-S Controller supports single register / memory access or burst access with address auto-increment capability.
- 7- or 10-bit addressing, General Call, SCL Low Wait States
- Digital filter for the received SDA and SCL lines
- Supports following I2C bus speeds:
    - Standard Mode (100 Kb/s)
    - Fast Mode (400 Kb/s)
    - Fast Mode plus (1 Mb/s)
    - Ultra Fast-Mode (5 Mb/s)
- Compliance with I2C specifications:
    - Philips – The I2C-Bus Specification, Version 2.1, January 2000
    - NXP UM10204 Rev 6 – 4 April 2014
- Fully-synchronous, synthesizable Verilog RTL core, with rising-edge clocking, no gated clocks, and no internal tri-states, for easy integration into FPGA or ASIC design flows.

Pin Description

The DB-I2C-S I2C Slave Controller interface signals are listed in Table 1.

Name	Type	Description
I2C Bus Interface		
SDAI	Input	Serial Data
SDAO	Output	Serial Data
SCLI	Input	Serial Clock Line
Global Reset, Clock		
RESETN	Input	Power-up Reset
CLK	Input	Clock
Register Array / SRAM / FIFO / AMBA / Avalon Interface		
Please contact Digital Blocks for more information		

Table 1: DB-I2C-S – I/O Pin Description

Verification Method

The DB-I2C-S Controller IP Core contains a test suite that generates & sends I2C transactions, monitors the I2C bus protocol, and checks expected results.

The DB-I2C-S Controller IP Core has internally been verified as follows:

- Instantiated within an FPGA, and communicating with NXP I2C Master IP Controller, and A NIOS II processor for expected data checking. I2C Bus Compliance testing with lab instrumentation.
- Instantiated within an FPGA, and communicating with Digital Blocks I2C Master IP Controller, and A NIOS II processor for expected data checking.

Customer Evaluation

Digital Blocks offers a variety of methods for prospective customers to evaluate the DB-I2C-S. Please contact Digital Blocks for additional information.

Deliverables

The DB-I2C-S is available in synthesizable RTL Verilog or a technology-specific netlist for FPGAs, along with Synopsys Design Constraints, a simulation test bench with expected results, datasheet, and user manual.

Ordering Information

Please contact Digital Blocks for additional technical, pricing, evaluation, and support information.

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