General Description

The Digital Blocks DB-DMAC-MC-AMBA is a Multi-Channel DMA Controller supporting 1 – 32 independent data block / packet / stream transfers. The Direct Memory Access (DMA) Controller IP Core contains 1 - 32 DMA Controller Engines (i.e. DMA Channels), supporting a 1 – 32 interfaces, including AMBA AXI / AHB / APB interconnects. A customized number of DMA Controller Engines and interfaces are available.

Figure 1 depicts the DMA Controller IP Core. The individual internal DMA Controller Engine services each interface at its maximum throughput, whether it's an AXI4 with high data burst and width capability, or Peripheral with slower speed, narrower data width requirements.

The DMA Controller IP Core can serve as a general-purpose Programmable DMA Controller supporting many system memories and peripherals, or be sized to the user required number of DMA Engines, AMBA interconnect interfaces, and user application interfaces.

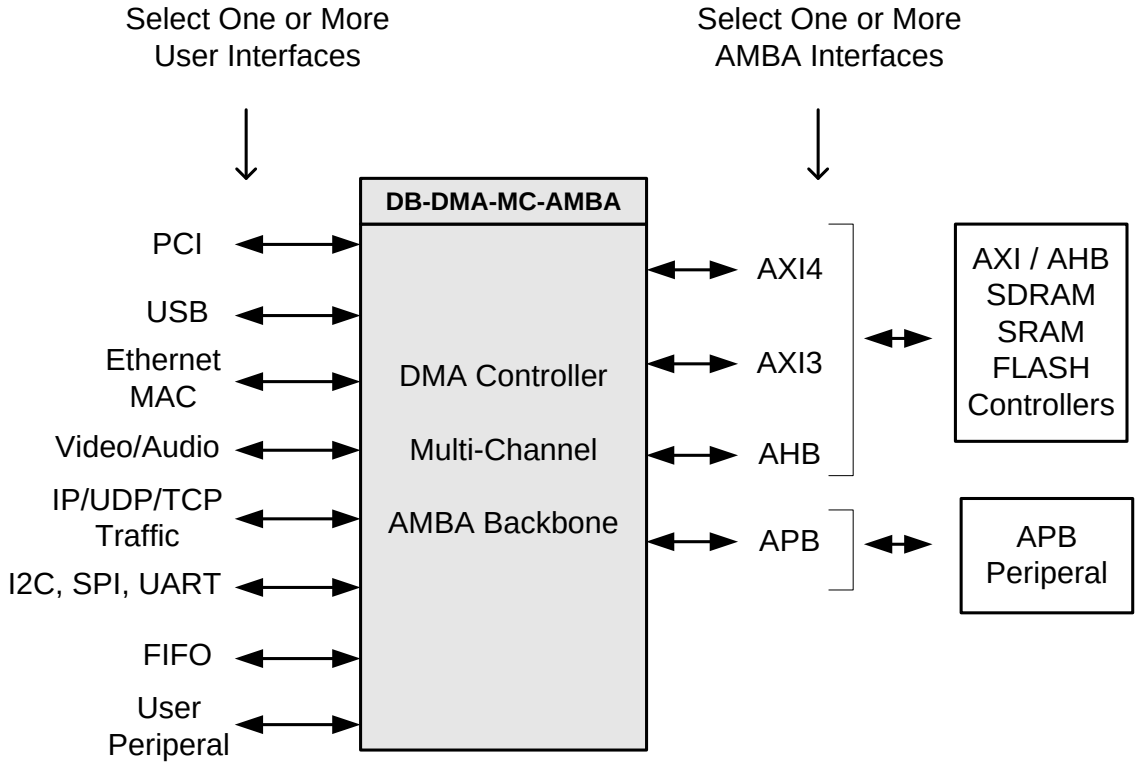

Figure 1: DB-DMA-MC-AMBA – DMA Controller - Multi-Channel

Features

- 1 - 32 Multi-Channel High Performance DMA Controller Engines:
    - High-Speed Finite State Machine Control
    - High Throughput to/from Memory & Peripherals via AMBA AXI / AHB on both small and large data sets
    - Dual-Port, Dual-Clock FIFO, user parameterized in Depth x Width
    - Optional Dual-Port, Single-Clock FIFO design
    - Optional Configurability via AMBA Slave Interface
- 1 – 32 User Port Interfaces
- Up to 32 DMA transfers in parallel active
- Hardware or Software Initiated Transfers
- Link-List Processor for Autonomous & Chained Block Transfers
- Arbiter with variety of Arbitration Modes including Quality of Service (QoS) and low-latency
- Individual Interface Data Widths: 8 / 16 / 32 / 64 / 128 / 256 / 512 / 1024. Data re-alignment matching interfaces with different data widths
- Programmable Data Burst Capability: 1, 4, 8, 16 on AXI3/AHB/User Interfaces. Up to 256 on AXI4
- Scatter / Gather – supports non-contiguous data block transfers to a contiguous segment of memory and vice versa
- Interrupt Controller – Signaling DMA Transfer Done & Diagnostics
- Fully-synchronous, synthesizable Verilog RTL core, with rising-edge clocking, no gated clocks, and no internal tri-states, for easy integration into FPGA or ASIC design flows.

Verification Method

The DB-DMAC-MC-AMBA DMA Controller IP Core contains a test suite that programs the Controller and sources and receives with checking data transfers.

The DB-DMAC-MC-AMBA DMA Controller IP Core has been implemented in a variety of Digital Blocks IP, including the LCD Controller, 2D Graphics Hardware Accelerator, and Low Latency / High-Speed Networking UDP/IP Protocol Stack Processor.

The DB-DMAC-MC-AMBA DMA Controller IP Core has been implemented in customer unique applications.

Customer Evaluation

Digital Blocks offers a variety of methods for prospective customers to evaluate the DB-DMAC-MC-AMBA DMA Controller IP Core. Please contact Digital Blocks for additional information.

Deliverables

The DB-DMAC-MC-AMBA is available in synthesizable RTL Verilog or a technology-specific netlist for FPGAs, along with Synopsys Design Constraints, a simulation test bench with expected results, datasheet, and user manual.

Ordering Information

Please contact Digital Blocks for additional technical, pricing, evaluation, and support information.

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