General Description

The Digital Blocks DB-DMAC-MC-AHB Verilog RTL IP Core is a DMA Controller targeting data transfer by 1-4 DMA Channels with respect 1-2 AMBA AHB Master Interfaces and 1-5 user defined peripheral interfaces. The IP Core contains an AHB Slave or APB Slave Interface for Configuration, Control, and Status as well as an Interrupt Controller for extensive diagnostics and reporting.

The DB-DMAC-MC-AHB is a fixed configuration of the DB-DMAC-MC-AMBA Multi-Channel DMA Controller, which contains 1 - 32 DMA Controller Engines (i.e. DMA Channels), supporting a 1 – 32 interfaces, including AMBA AXI / AHB / APB interconnects.

Figure 1 depicts the DMA Controller IP Core. The individual internal DMA Controller Engines (i.e. each DMA Channel) services each interface at its maximum throughput, whether it's an AHB with high data burst and width capability, or a Peripheral with slower speed, narrower data width requirements.

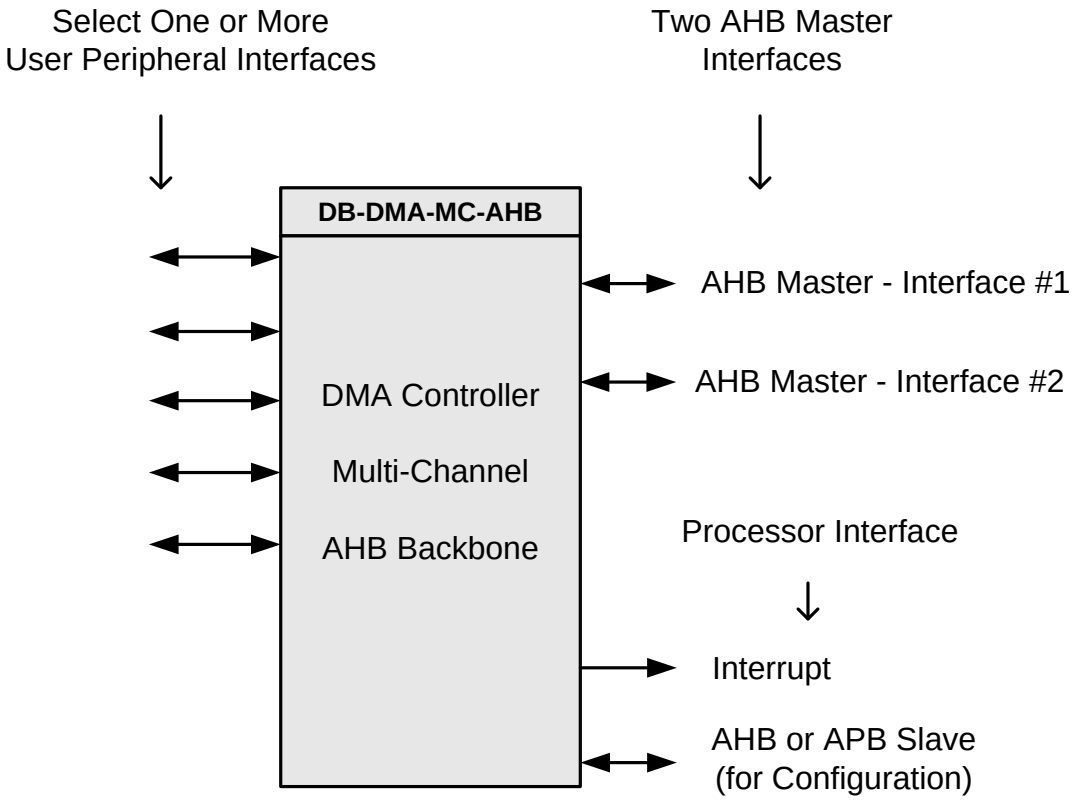

Figure 1: DB-DMA-MC-AHB – DMA Controller – AHB Multi-Channel

Features

- 1 - 4 Multi-Channel High Performance DMA Controller Engines:
  - High-Speed Finite State Machine Control
  - High Throughput to/from Memory & Peripherals via AMBA AHB on both small and large data sets
  - Configurable with Dual-Port, Single- or Dual-Clock FIFO
  - FIFOs user parameterized in Depth x Width
  - User program Control, Status, Diagnostics via AMBA AHB/APB Slave Interface
  - Scatter / Gather – supports non-contiguous data block transfers to a contiguous segment of memory and vice versa
- Scatter Gather List (SGL) –
  - processing of linked-list Descriptor nodes
  - supports non-contiguous data block transfers to a contiguous segment of memory and vice versa
- Targets PCIe or CPU DMA Controller in Linux environment
- 1 – 2 AHB Master Interfaces
  - Individual Interface Data Widths: 8 / 16 / 32 / 64 / 128 / 256 / 512 / 1024. Data re-alignment matching interfaces with different data widths
  - Programmable Data Burst Capability: 1, 4, 8, 16 on AHB/User Interfaces.
- 1 – 5 User Peripheral Port Interfaces
- Variety of User DMA Transfer Control:
  - Hardware or Software Initiated Transfers
  - Link-List Processor for Autonomous & Chained Block Transfers
- Arbiter with variety of Arbitration Modes
- Interrupt Controller – Signaling DMA Transfer Done & Diagnostics
- Fully-synchronous, synthesizable Verilog RTL core, with rising-edge clocking, no gated clocks, and no internal tri-states, for easy integration into FPGA or ASIC design flows.

Verification Method

The DB-DMAC-MC-AHB DMA Controller IP Core contains a test suite that programs the Controller and sources and receives with checking data transfers.

The DB-DMAC-MC-AHB DMA Controller IP Core has been implemented in a variety of Digital Blocks IP, including the LCD Controller, 2D Graphics Hardware Accelerator, and Low Latency / High-Speed Networking UDP/IP Protocol Stack Processor.

The DB-DMAC-MC-AHB DMA Controller IP Core has been implemented in customer unique applications.

Customer Evaluation

Digital Blocks offers a variety of methods for prospective customers to evaluate the DB-DMAC-MC-AHB DMA Controller IP Core. Please contact Digital Blocks for additional information.

Deliverables

The DB-DMAC-MC-AHB is available in synthesizable RTL Verilog or a technology-specific netlist for FPGAs, along with Synopsys Design Constraints, a simulation test bench with expected results, datasheet, and user manual.

Ordering Information

Please contact Digital Blocks for additional technical, pricing, evaluation, and support information.

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