Digital Blocks   DB-AXI4-STREAM-TO-AXI4-MM

Semiconductor IP   AXI4-Stream to AXI4 Memory Map Bridge

General Description

The Digital Blocks DB-AXI4-STREAM-TO-AXI4-MM-BRIDGE Verilog RTL IP Core accepts AXI4-Stream data and control input, converts the control TID to a AXI4 Memory Map address, and signals a DMA Controller to read the data by way of a AXI4 Slave Memory Map read channel.

The Digital Blocks DB-AXI4-STREAM-TO-AXI4-MM-BRIDGE IP Core works with Digital Blocks DMA Controller (i.e. the DB-DMAC-MC-AXI Verilog RTL IP Core) to transfer data from an AXI4-Stream peripheral or AXI4-Stream Network Interface to either memory or another peripheral.

Digital Blocks companion IP, the DB-AXI4-MM-TO-STREAM-BRIDGE, works with Digital Blocks DMA Controller to transfers data from memory or a peripheral to an AXI4-Stream peripheral or AXI4-Stream Network Interface.

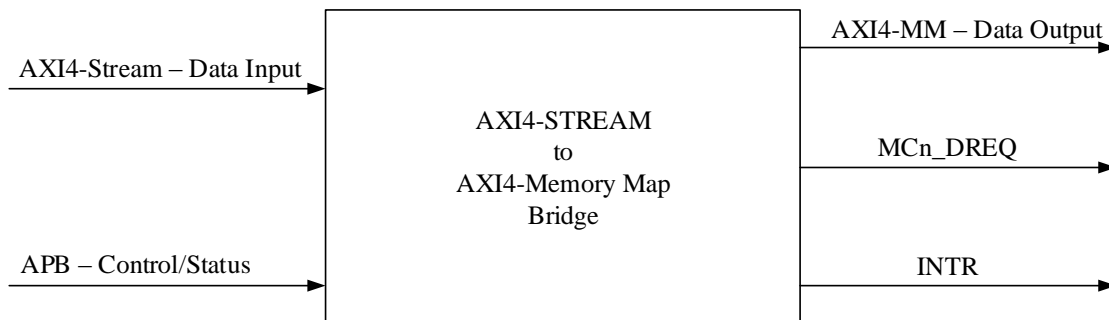Figure 1 depicts DB-AXI4-STREAM-TO-AXI4-MM-BRIDGE Verilog IP Core.

Figure 1: DB-AXI4-STREAM-TO-AXI4-MM-BRIDGE – Top Level View

Features

- Converts AXI4-Stream Interface to AXI4/AXI3 Memory Map Data & Control Interface
    - o Standard release supports 16 AXI4-Stream Channels.
    - o More or less Channels optional. Contact Digital Blocks with requirements.
- Works with Digital Blocks DMA Controller to support following data transfers:
    - o Peripheral-to-Memory
    - o Peripheral-to-Peripheral
    - o Network-to-Memory
    - o Network-to-Peripheral
- Individual Interface Data Widths: 8 / 16 / 32 / 64 / 128 / 256 / 512 / 1024.
- Interrupt Controller – for Diagnostics
- Fully-synchronous, synthesizable Verilog RTL core, with rising-edge clocking, no gated clocks, and no internal tri-states, for easy integration into FPGA or ASIC design flows.

Verification Method

The DB-AXI4-STREAM-TO-AXI4-MM-BRIDGE IP Core contains a test suite that programs the IP and sources and receives data with checking results.

The DB-AXI4-STREAM-TO-AXI4-MM-BRIDGE Controller IP Core has been implemented in customer unique applications.

Customer Evaluation

Digital Blocks offers a variety of methods for prospective customers to evaluate the DB-AXI4-STREAM-TO-AXI4-MM-BRIDGE Controller IP Core. Please contact Digital Blocks for additional information.

Deliverables

The DB-AXI4-STREAM-TO-AXI4-MM-BRIDGE is available in synthesizable RTL Verilog or a technology-specific netlist for FPGAs, along with Synopsys Design Constraints, a simulation test bench with expected results, datasheet, and user manual.

Ordering Information

Please contact Digital Blocks for additional technical, pricing, evaluation, and support information.

Digital Blocks, Inc.
PO Box 192
587 Rock Rd
Glen Rock, NJ 07452 USA
Phone: +1-201-251-1281
eFax: +1-702-552-1905
info@digitalblocks.com